1   two pairs of linear feedback shift registers, wherein second seed values for the second

2   pair of linear feedback shift registers are different from first seed values for the first pair of

3   linear feedback shift registers, the second seed values being calculated from the first seed

4   values, wherein the first and second pair of linear feedback shift registers are implemented to

5   produce more than one new state bit and more than one output bit for each linear feedback

6   shift registers at the same time.

1   2. (Original) The gold code generator of claim 1 wherein the seed values for the second pair of

2   linear feedback shift registers are delayed values of the first seed values.

1   3. (Previously amended) The gold code generator of claim 1 wherein the gold code generator is

2   implemented on a reconfigurable ~~logic~~ chip.

1   4. (Original) The gold code generator of claim 3 wherein the calculation of some of the second

2   seed values is done using a dedicated processor on the reconfigurable chip.

1   5. (Original) The gold code generator of claim 3 wherein the gold code generator configuration is

2   loaded into a background plane of the reconfigurable chip, while the reconfigurable chip is

3   operating on another configuration in the foreground.

1   6. (Original) The gold code generator of claim 3 wherein the feedback is implemented using

2   lookup tables.

1   7-11. (previously canceled).

1   12. (Original) A method of implementing a pseudo-random code generator:

2   converting a psuedo-random code generator specification into an equivalent

3   representation, the psuedo-random code generator specification being such that taps used to

4   calculate an output include at least one tap within n spaces from the input, the equivalent

5   representation is such that no such taps are within n spaces from the input; and

6   implementing the equivalent representation such that multiple new state bits are

7   calculated at the same time.

1   13. (Currently Amended) The method of claim 12 wherein the pseudo-random code generator

2   specification being such that taps to calculate an output is defined within a first ~~chip~~ shift

3   register span, the equivalent representation is such that taps to calculate an output bit are

4   within a smaller shift register span.

1   14. (Original) The method of claim 12 wherein the equivalent representation includes two pairs

2   of linear feedback shift registers wherein the second seed values for the second pair of linear

3   feedback shift registers is different from a first seed value for the first pair of linear feedback

4   shift registers.

1   15. (Original) The method of claim 12 wherein the pseudo-random code generator comprises a

2   gold code generator.

1   16. (Original) The method of claim 12 wherein the pseudo-random code generator is

2   implemented on a reconfigurable chip.

1   17. (Original) A method of implementing a pseudo-random code generator comprising:

2   converting a pseudo-random code generator specification into an equivalent

3   representation, the psuedo-random code generator specification being such that taps to

4   calculate an output are defined within a first shift register span, the equivalent representation

5   is such that the taps to calculate an output bit are within a smaller shift register span; and

6   implementing the equivalent representation such that multiple output bits are calculated

7   at the same time.

1   18. (Original) The method of claim 17 wherein the pseudo-random code generation specification

2   is such that taps used to calculate an output have at least one tap within n spaces from the

3   input, the equivalent representation is such that no such tap is within n spaces from the input.

1   19. (Original) The method of claim 17 wherein two pairs of linear feedback shift registers are

2   used in the equivalent representation.

1   20. (Original) The method of claim 19 wherein the second seed values for the second pair of

2   linear feedback shift registers are different from the first seed values for the first pair of linear

3   feedback shift registers.

1   21. (Original) The method of claim 17 implemented on a reconfigurable chip.

1   22. (Original) The method of claim 17 wherein in the equivalent representation of the output bits

2   are calculated from taps at a single register for each linear feedback shift register.

1·   23. (Previously Added) A system comprising:

2   a gold code generator, wherein the gold code generator comprises multiple pairs of linear

3   feedback shift registers implemented to simultaneously produce more than one state bit and

4   more than one output bit for each linear feedback shift registers;

5   at least one reconfigurable chip where reconfigurable elements are selectively configured

6   by at least the output of the gold code generator; and

7   a communication element, coupled with the reconfigurable chip, to receive output from

8   the at least one reconfigurable chip to enable wireless communication.

1   24. (Previously Added) The system of claim 23 wherein the gold code generator configuration is

2   loaded into a background plane of the at least one reconfigurable chip, while the at least one

3   reconfigurable chip is operating on another configuration in a foreground plane, wherein

4   once the gold code generator is loaded into the background plane, the gold code generator

5   configuration can be activated to produce an output, at least a subset of which is used to

6   reconfigure the at least one reconfigurable chip.

1   25. (Previously Added) The system of claim 24 wherein the configuration in the foreground

2   plane

3   is an other gold code generator configuration.

1   26. (Previously Added) The system of claim 23 wherein a seed value for a first pair of linear

2   feedback shift registers are different from a seed value for other pairs of linear feedback shift

3   registers.

1`   27. (Previously Added) The system of claim 26 wherein a subsequent seed value is calculated

2   from

3   the first seed value.

1   28. (Previously Added) The system of claim 27 wherein the calculation of the subsequent seed

2   value is done at least partially in a processor on the at least one reconfigurable chip.

1   29. (Previously Added) The system of claim 23 wherein the gold code generator is implemented

2   on an at least one reconfigurable chip.

1   30. (Previously Added) The system of claim 23 wherein the communication element is a

2   transmitter for spread spectrum transmission.

1   31. (Previously Added) The system of claim 23 wherein the communication element is a receiver

2   for spread spectrum reception.

1   32. (Previously Added) A gold code generator comprising:

2   multiple pairs of linear feedback shift registers to simultaneously produce more than one

3   state bit and more than one output bit for each pair of linear feedback shift registers.

1   33. (Previously Added) The gold code generator of claim 32 wherein the gold code generator is

2   implemented on a reconfigurable chip.

1   34. (Previously Added) The gold code generator of claim 33 wherein the gold code generator

2   configuration is loaded into a background plane of the reconfigurable chip, while the

3   reconfigurable chip is operating on another configuration in a foreground plane.

1   35. (Previously Added) The gold code generator of claim 33 wherein feedback is implemented

2   using lookup tables.

1   36. (Previously Added) The gold code generator of claim 32 wherein a seed value for the gold

2   code generator for a first pair of linear feedback shift registers are different from a seed value

3   for other pairs of linear feedback shift registers.

1   37. (Previously Added) The gold code generator of claim 36 wherein the seed value for the other

2   pairs of linear feedback shift registers is calculated from the first seed value.

1   38. (Previously Added) The gold code generator of claim 36 wherein the calculation of the seed

2   value for the other pairs of linear feedback shift registers is done at least partially in a

3   processor on the reconfigurable chip.